Article ID: 1000-7032(2012)11-1258-06

The Stability of IGZO-TFT with Reactive Sputtered SiO_x Insulator under White Light Illumination

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Abstract: We systematically investigated the stability of gallium indium zinc oxide (IGZO) thin film transistor (TFT) with reactive sputtered SiO_x insulator under white light illuminaion. The research involved an overall stress conditions that included light stress (LS), negative voltage stress (NBS), positive voltage stress (PBS), negative bias-light stress (NBLS), and positive bias-light stress (PBLS). The results demonstrate a large threshold voltage shift under LS and NBLS conditions, and a negligible threshold voltage shift under PBLS condition. The *C-V* characteristics indicated that the shift of threshold voltage came from traps generated at or near the dielectric/semiconductor interface. Additionally, the stretched exponential model was used to obtain the relaxation time. This work aimed to provide an instability origin of IGZO-TFT under white light illumination and gate voltage bias.

Key words: thin film transistor; stability; reactive sputtered SiO_x
CLC number: O472.4 **Document code**: A **DOI**: 10.3788/fgxb20123311.1258

用反应溅射法沉积 SiO_x 绝缘层的 InGaZnO-TFT 的光照稳定性

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摘要: 制备了基于反应溅射 SiO_x 绝缘层的 InGaZnO-TFT,并系统地研究了 InGaZnO-TFT 在白光照射下的稳定性,主要涉及到光照、负偏压、正偏压、光照负偏压和光照正偏压5种情况。结果表明,器件在光照和负偏压光照下的阈值偏移较大,而在正偏压光照情况下的阈值偏移几乎可以忽略。采用 *C-V* 方法证明阈值电压漂移是源于绝缘层/有源层附近及界面处的缺陷。另外,采用指数模式计算了缺陷态的弛豫时间。本研究的目的就是揭示 InGaZnO-TFT 在白光照射和偏压下的不稳定的原因。

关 键 词: 薄膜晶体管; 稳定性; 反应溅射 SiO_x

收稿日期: 2012-07-01; **修订日期**: 2012-09-20
基金项目: 国家自然科学基金(61274082,61077013,60777018,60776040); 国家"863"计划(2010AA3A337, 2008AA03A336); 中国博士后基金(2012T50387,2011M500569)资助项目
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1 Introduction

Gallium indium zinc oxide (IGZO) thin film transistors (TFTs) have received much attention due to their potential application in active matrix liquid crystal displays (AM-LCDs), and active matrix organic light emitting diodes (OLEDs)[1-4]. Recently, the mobility of IGZO-TFT has improved significantly and reached a value of more than 5 $cm^2 \cdot V^{-1} \cdot s^{-1}$[5]. Although the mobility of IGZO-TFT is acceptable, the poor stability of IGZO-TFT is becoming a restricting factor in practical application. Some groups have studied the stability of IGZO-TFT under constant positive/negative gate bias[6-7]. However, in a real working AMLCD panel, the devices are inevitably exposed to white light illumination emanating from the backlight unit, and the switching TFTs always adopt a negative gate bias to maintain the "off" state of the pixel, thus it is necessary to maintain the stability under negative bias-light stress. In addition, the driving TFTs operate for a long period under simultaneous application of a positive gate bias and light illumination, so it is also important to study the stability under positive bias-light stress. Some studies have already reported the effect of illumination on amorphous IGZO-TFT under bias stress[8-9]. However, a systematic study is rather sparse. Because it involves an overall stress condition including light stress (LS), negative voltage stress (NBS), positive voltage stress (PBS), negative bias-light stress (NBLS), and positive bias-light stress (PBLS). Furthermore, few reports are quantitatively explained the origin of instability using *C-V* method.

In this work, IGZO-TFT with reactive sputtered SiO_x insulator under the different stress conditions (LS, NBS, PBS, NBLS, and PBLS) has been examined. The origin of instability is analyzed using the high-frequency (1 MHz) normalized *C-V* measurements of the IGZO MIS capacitors.

2 Experiments

The cross section of the IGZO-TFT was shown schematically in Fig. 1. Prior to the different SiO_x films deposition on ITO glass, the ITO glass was cleaned with acetone, ethanol, and de-ionized water in that order. The sheet resistance of the ITO film was 30 Ω/□. Reactive sputtered SiO_x film was deposited at room temperature with a mixture of high purity Ar and O_2 (Ar/O_2 flow ratio of 65/35). The target was Si (99.99%, 5.08 cm(2 in)). The forward power was kept at 100 W and the chamber pressured was held at 0.6 Pa. Following this, 40 nm of IGZO was deposited at room temperature via radio frequency (RF) magnetron sputtering to form the active layer. The sputtering was carried out in an argon (Ar) atmosphere at 1.2 Pa and a power of 50 W using a ceramic IGZO target (n(In)∶n(Ga)∶n(Zn) = 1∶1∶1, molar ratio). A 60-nm-thick Al film was sequentially vacuum deposited onto IGZO layer using a metal mask to define transistors with channel width W = 1 000 μm and channel length L = 180 μm. Finally, the sample was subjected to thermal annealing at 250 ℃ for 30 min.

The current-voltage characteristics of the devices were measured by using an Agilent E3647A Dual output DC power supply and a Keithley 6485 Picoammeter. The capacitance measurements were conducted with a HP 4284A Precision LCR meter. The thickness of SiO_x gate insulator was determined by a surface profiler (Alpha-Step IQ). All measurements were carried out in air ambiance at room temperature.

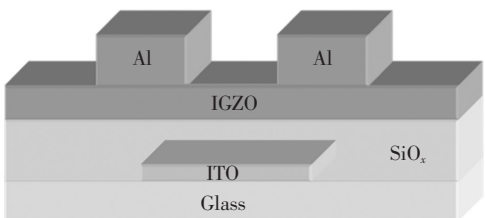

Fig. 1　Schematic structure of the IGZO-TFT

3 Results and Discussion

Fig. 2 (a), (b) and (c) are the transfer characteristics of devices subjected to light stress (LS), positive bias-light stress (PBLS) and negative bias-light stress (NBLS), respectively. A white light intensity of 10 000 lx is performed for 2 h, and the positive and negative bias stress are +10 V and

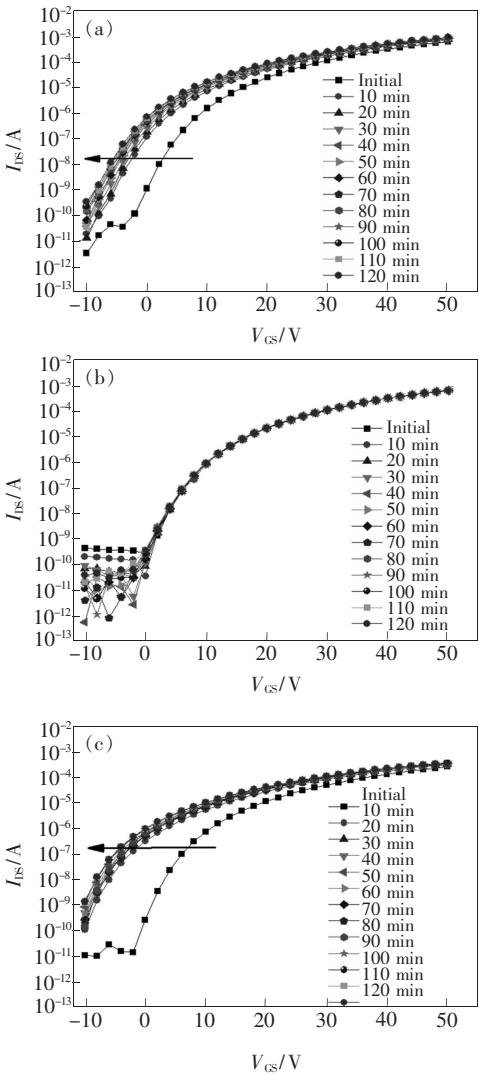

Fig. 2 Transfer characteristics of IGZO-TFT subjected to 10 000 lx white light illumination under (a) without gate bias stress, (b) 10 V gate bias stress, and (c) −10 V gate bias stress.

−10 V, respectively. V_{GS} is swept from −10 V to +50 V with the application of V_{DS} = 30 V. The saturation mobility (μ_{sat}) is extracted from a linear fitting to the $(I_{DS})^{1/2}$-V_{GS} curve, based on the equation $I_{DS} = (\mu_{sat} C_{ox} W/2L)(V_{GS} - V_{th})^2$, where V_{th} is the threshold voltage estimated from the intercept of the extrapolated curve with the voltage axis. The initial performance of the device without illumination is characterized in the dark environment. The device exhibits excellent electrical properties of μ_{sat} = 18.7 $cm^2 \cdot V^{-1} \cdot s^{-1}$, V_{th} = 15.3 V, and $I_{on}/I_{off} = 1.8 \times 10^8$. During illumination, the threshold voltage shifts to more negative direction with the increasing illumination time. After 7 200 s continuous illumination with a 10 000 lx white light, the μ_{sat} and V_{th} value are reduced to 15.6 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and 7.1 V, respectively. From Fig. 2 (a), it is easily seen that the I_{off} value increases with the increase of illumination time due to more photo-generated charges. The device shows a large negative V_{th} shift about −8.2 V after 7 200 s white light illumination, and the tendency of V_{th} shift increases gradually with increasing illumination time. Recently, T. C. Chen *et al*[10] have reported a plausible mechanism for the V_{th} instability under illumination condition, in which the holes generated from light induced electron-hole pairs that react with the preabsorbed O_2^- to reduce into O_2, resulting in a negative V_{th} shift. Compared with the transfer characteristics under LS condition, the threshold voltage of the device under NBLS shows a smaller value. However, the device under PBLS condition shows a better stability than that under LS condition. The saturation mobility of the device under PBLS almost remains unchanged.

To further probe the instability of IGZO-TFT with reactive sputtered SiO_x insulator, Fig. 3 compares the threshold voltage shift of devices subjected to light stress (LS), negative voltage stress (NBS), positive voltage stress (PBS), negative bias-light stress (NBLS), and positive bias-light stress (PBLS). After gate bias stress for 7200 s, a positive shift of ($\Delta V_{th} \approx 1.8$ V) for positive gate bias stress (V_{GS} = 10 V) and a negative shift ($\Delta V_{th} \approx -2$ V) for negative gate bias stress (V_{GS} = −10 V) are obtained. The application of positive/negative bias stress to the gate causes redistributions in the trapped charge of the active layer in the IGZO-TFT. The device under NBLS condition shows a large V_{th} shift of −9.7 V, which is much larger than V_{th} shift of the device under NB condition. When a negative gate voltage (V_{GS} = −10 V) is applied under illumination conditions, the illumination induces photo-excitation of valence band electrons into midgap states. Simultaneously, it will generates free hole carriers in the valence. Such free holes in the valence band will be attracted to the SiO_x/IGZO interface by the negative gate field and become trapped at

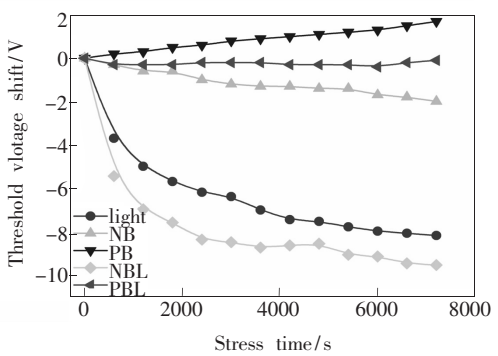

Fig. 3　Graph of the threshold voltage shift with respect to stress time

the interfacial energy states or injected into the SiO_x layer leading to negative V_{th} shift of the IGZO-TFT.

The schematic band diagram is shown in Fig. 4 (a). Negative stress depletes the trapped charge between E_F and the conduction band, causing the Fermi level to be slightly shifted towards the conduction band. Therefore, the application of V_{GS} easily shifts the E_F to the conduction band, remaining fixed by the band-tail states. However, when the positive bias stress is applied under the same light illumination, the threshold voltage shift of IGZO-TFT under PBLS condition is only −0.2 V, which is much smaller than that of IGZO-TFT under LS condition (−9.5 V). It illustrates that the positive bias stress can suppress the negative V_{th} shift. On the contrary, the illumination can suppress the positive V_{th} shift. It suggests that the generated electron in the channel layer drifts toward the channel/insulator interface under the positive voltage and accumulated near the interface. At the same time, the positive gate field repels most of the photo-generated holes away from the gate insulator. The electrons and positive charges newly generated by light illumination under the positive gate bias seem to recombine very quickly under high drain-source current, as shown in Fig. 4(b), resulting in less V_{th} shift. Similar results have been reported by other groups[11]. It also verifies the fact

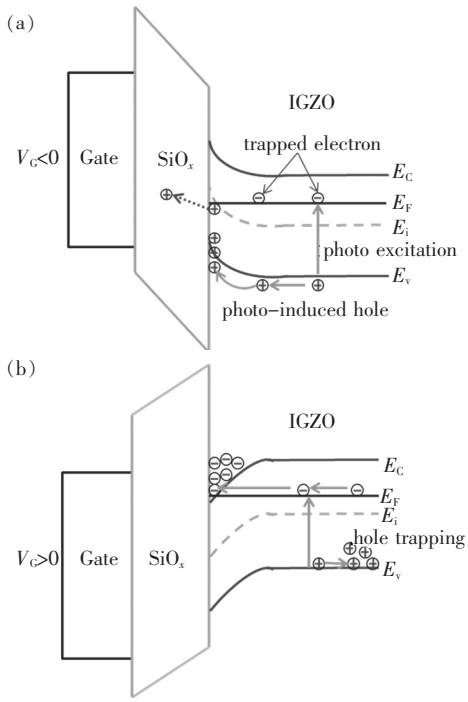

Fig. 4　Energy band diagrams of the IGZO-TFT under (a) negative bias-light stress, and (b) positive bias-light stress.

that illumination can excite the trapped charges and accelerated the charge de-trapping process[12].

The relationship between ΔV_{th} and t is found to fit the stretched exponential model, which is originated from the negative charge being trapped at the channel/dielectric interface or getting injected into the gate dielectric[13-14]. A stretched exponential model can be described by the following equation:

$$|\Delta V_{th}(t)| = |V_0|\left\{1-\exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right]\right\}, \quad (1)$$

where $V_0 = V_{GS} - V_{th,0}$, $V_{th,0}$ is the threshold voltage at the start of the stress measurement. β is the stretched exponential exponent, and τ reflects the characteristics carrier trapping time. The associated parameters are list in Table 1. The parameters indicate that carriers are easily injected into the gate insulator at the semiconductor/dielectric interface for

Table 1　Stretched exponential parameters under the different stress conditions

Parameters	NBS	PBS	LS	NBLS	PBLS
τ/s	1.05×10^5	6.8×10^5	8.6×10^3	7.6×10^3	3.5×10^6
β	0.746	0.812	0.495	0.286	0.149

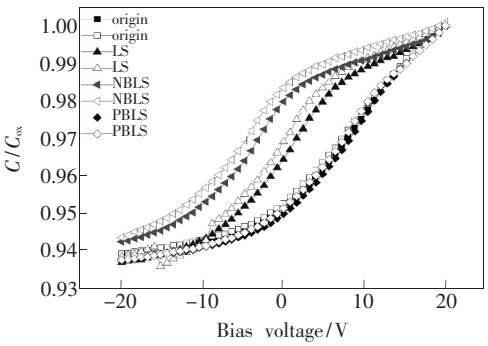

Fig. 5 Normalized *C-V* measurements of IGZO MIS capacitors under different stress

device under the negative bias illumination stress.

To further explain the charge trapping phenomenon, the high-frequency (1 MHz) normalized *C-V* measurements of the IGZO MIS capacitors with reactive sputtered SiO_x is shown in Fig. 5. The voltage V_G is swept from 20 V to −20 V and back to 20 V. A small and negligible hysteresis is observed for the device under positive bias-light stress or dark condition. However, the hysteresis width of $\Delta V_G = 1.2$ V is obtained for device under light stress. For the device under negative bias-light stress, the hysteresis width shows a bigger value of $\Delta V_G = 1.8$ V. The charge-trapping density (N_t) can be calculated by using the relation: $N_t \backsimeq [C_i(\Delta V_G)/q]$, where C_i is the gate insulator capacitance and q is the elementary charge. The value of charge trapping is estimated to be 7.5×10^{10} and 1.1×10^{11} cm^{-2} for the device under light stress and negative bias-light stress, respectively. It illustrates that the hysteresis effect may be attributed to the increasing of charges at/near IGZO/SiO_x interface or bulk trap under LS or NBLS condition.

4 Conclusion

In conclusion, the IGZO-TFT with reactive sputtered SiO_x insulator under the different stress conditions (LS, NBLS, and PBLS) has been examined. Light stress leads to a negative threshold voltage shift. Compared with the threshold voltage shift under LS, the threshold voltage shifts under NBLS and PBLS are deteriorated and suppressed. *C-V* characteristics verifies that the instability of the device is attributed to the increasing of charges at/near IGZO/SiO_x interface or bulk trap under light stress or negative bias-light stress.

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